

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1       1. (Currently Amended) A method of exporting emulation  
2 information from a data processor, comprising:

3       collecting internal emulation information ~~within~~ from a data  
4 processor;

5       arranging the collected emulation information into a plurality  
6 of first information blocks having a first fixed size;

7       receiving the plurality of first information blocks and  
8 arranging the emulation information contained therein into a  
9 plurality of second information blocks having a second fixed size  
10 which ~~differ in size~~ differs from the first fixed size of the first  
11 information blocks; and

12       outputting a sequence of the second information blocks ~~from~~  
13 ~~the data processor~~ via a plurality of terminals ~~of the data~~  
14 ~~processor~~ equal in number to said second fixed size.

1       2. (Currently Amended) The method of Claim 1, wherein the  
2 second ~~information blocks are~~ fixed size is smaller in size than  
3 the first ~~information blocks~~ fixed size.

1       3. (Original) The method of Claim 1, including receiving the  
2 sequence of second information blocks externally of the data  
3 processor, and re-arranging the emulation information contained in  
4 the second information blocks into a plurality of the first  
5 information blocks.

1       4. (Original) The method of Claim 1, wherein each of the  
2 first and second information blocks is a packet of emulation  
3 information.

Claims 5 to 15. (Cancelled)

1 16. (Currently Amended) An integrated circuit, comprising:  
2 a data processor for performing data processing operations;  
3 a collector coupled to said data processor for collecting  
4 emulation information from said data processor and arranging said  
5 emulation information into a plurality of first information blocks  
6 having a first fixed size;  
7 an exporter coupled to said collector for receiving therefrom  
8 said plurality of first information blocks and arranging said  
9 emulation information contained therein into a plurality of second  
10 information blocks having a second fixed size which differ in size  
11 differs from the first fixed size of said first information blocks;  
12 a plurality of terminals for outputting information equal in  
13 number to said second fixed size; and  
14 said exporter coupled to said terminals for outputting a  
15 sequence of the second information blocks via said terminals.

1 17. (Currently Amended) The integrated circuit of Claim 16,  
2 wherein said second information blocks are fixed size is smaller in  
3 size than said first information blocks fixed size.

Claims 18 to 26. (Cancelled)

1 27. (Currently Amended) A data processing system, comprising:  
2 an integrated circuit, including a data processor for  
3 performing data processing operations;  
4 an emulation controller coupled to said integrated circuit for  
5 controlling emulation operations of said data processor;  
6 said integrated circuit including an apparatus coupled between  
7 said data processor and said emulation controller for providing

8 emulation information about said data processing operations, said  
9 apparatus including a collector coupled to said data processor for  
10 collecting said emulation information from said data processor and  
11 arranging said emulation information into a plurality of first  
12 information blocks having a first fixed size, and an exporter  
13 coupled to said collector for receiving plurality of first  
14 information blocks and arranging said emulation information  
15 contained therein into a plurality of second information blocks  
16 having a second fixed size which differ in size differs from the  
17 first fixed size of said first information blocks; and

18 said integrated circuit including a plurality of terminals  
19 coupled to said emulation controller equal in number to said second  
20 fixed size for outputting information to said emulation controller,  
21 said exporter coupled to said terminals for outputting a sequence  
22 of said second information blocks to said emulation controller via  
23 said terminals.

1 28. (Original) The system of Claim 27, including a  
2 man/machine interface coupled to said emulation controller for  
3 permitting a user to communicate with said emulation controller.

1 29. (Original) The system of Claim 28, wherein said  
2 man/machine interface includes one of a visual interface and a  
3 tactile interface.

1 30. (New) The method of Claim 2, wherein:  
2 said first fixed size is an integral multiple of said second  
3 fixed size; and  
4 said step of receiving the plurality of first information  
5 blocks and arranging the emulation information contained therein  
6 into a plurality of second information blocks includes the steps of

(a) storing a current first information block in a current packet register,

(b) sequentially selecting groups of the second fixed size bits from the current packet register as a second information block, a first selected group beginning at a first bit of said current packet register, subsequent selected groups beginning at a bit following a last bit of a prior group, until all bits of the current packet register are selected,

(c) thereafter storing a next first information block in the current block register and repeating steps (a), (b) and (c).

31. (New) The method of Claim 2, wherein:

said first fixed size is not an integral multiple of said  
and fixed size; and

said step of receiving the plurality of first information blocks and arranging the emulation information contained therein into a plurality of second information blocks includes the steps of

(a) storing a current first information block in a current packet register,

(b) sequentially selecting groups of the second fixed size bits from the current packet register as a second information block, a first selected group beginning at a next bit of said current packet register, subsequent selected groups beginning at a bit following a last bit of a prior group, until a number of bits of remaining in the current packet register is less than the second fixed number,

(c) storing the current first information block in a last packet register,

(d) storing a next first information block in the current packet register,

20 (e) selecting a group of the second fixed size bits from  
21 a set of bits remaining in the last packet register and bits  
22 starting at a first bit of the current packet register, and  
23 (f) thereafter repeating steps (b), (c), (d) and (e).

1           32. (New) The integrated circuit of claim 17, wherein:  
2            said first fixed size is an integral multiple of said second  
3            fixed size; and  
4            said exporter includes  
5            a current packet register, and  
6            a combiner connected to said current packet register and  
7            said terminals, said combiner operable to  
8            (a) store a current first information block in a  
9            current packet register,  
10           (b) sequentially select groups of the second fixed  
11           size bits from the current packet register as a second  
12           information block, a first selected group beginning at a  
13           first bit of said current packet register, subsequent  
14           selected groups beginning at a bit following a last bit  
15           of a prior group, until all bits of the current packet  
16           register are selected,  
17           (c) thereafter store a next first information block  
18           in the current block register and repeat steps (a), (b)  
19           and (c).

1       33. (New) The integrated circuit of claim 17, wherein:  
2       said first fixed size is not an integral multiple of said  
3       second fixed size; and  
4       said exporter includes  
5            a current packet register,  
6            a last packet register, and

7           a combiner connected to said current packet register and  
8        said terminals, said combiner operable to

9               (a) store a current first information block in a  
10      current packet register,

11               (b) sequentially select groups of the second fixed  
12      size bits from the current packet register as a second  
13      information block, a first selected group beginning at a  
14      next bit of said current packet register, subsequent  
15      selected groups beginning at a bit following a last bit  
16      of a prior group, until a number of bits of remaining in  
17      the current packet register is less than the second fixed  
18      number,

19               (c) store the current first information block in a  
20      last packet register,

21               (d) store a next first information block in the  
22      current packet register,

23               (e) select a group of the second fixed size bits  
24      from a set of bits remaining in the last packet register  
25      and bits starting at a first bit of the current packet  
26      register, and

27               (f) thereafter repeat steps (b), (c), (d) and (e).

1       34. (New) The data processing system of Claim 27, wherein:  
2        said second fixed size is smaller in size than said first  
3       fixed size.

1       35. (New) The data processing system of claim 34, wherein:  
2        said first fixed size is an integral multiple of said second  
3       fixed size; and

4        said exporter includes  
5        a current packet register, and

6           a combiner connected to said current packet register and  
7        said terminals, said combiner operable to

8           (a) store a current first information block in a  
9        current packet register,

10          (b) sequentially select groups of the second fixed  
11        size bits from the current packet register as a second  
12        information block, a first selected group beginning at a  
13        first bit of said current packet register, subsequent  
14        selected groups beginning at a bit following a last bit  
15        of a prior group, until all bits of the current packet  
16        register are selected,

17          (c) thereafter store a next first information block  
18        in the current block register and repeat steps (a), (b)  
19        and (c).

1        36. (New) The data processing system of claim 34, wherein:  
2        said first fixed size is not an integral multiple of said  
3        second fixed size; and

4        said exporter includes

5        a current packet register,

6        a last packet register, and

7        a combiner connected to said current packet register and  
8        said terminals, said combiner operable to

9           (a) store a current first information block in a  
10        current packet register,

11          (b) sequentially select groups of the second fixed  
12        size bits from the current packet register as a second  
13        information block, a first selected group beginning at a  
14        next bit of said current packet register, subsequent  
15        selected groups beginning at a bit following a last bit  
16        of a prior group, until a number of bits of remaining in

17           the current packet register is less than the second fixed  
18           number,  
19               (c) store the current first information block in a  
20           last packet register,  
21               (d) store a next first information block in the  
22           current packet register,  
23               (e) select a group of the second fixed size bits  
24           from a set of bits remaining in the last packet register  
25           and bits starting at a first bit of the current packet  
26           register, and  
27               (f) thereafter repeat steps (b), (c), (d) and (e).